MICROPROCESSOR AND ASSEMBLY LANGUAGE

PROGRAMMABLE INTERRUPT CONTROLLER

PROGRAMMABLE INTERRUPT CONTROLLER(8259A)

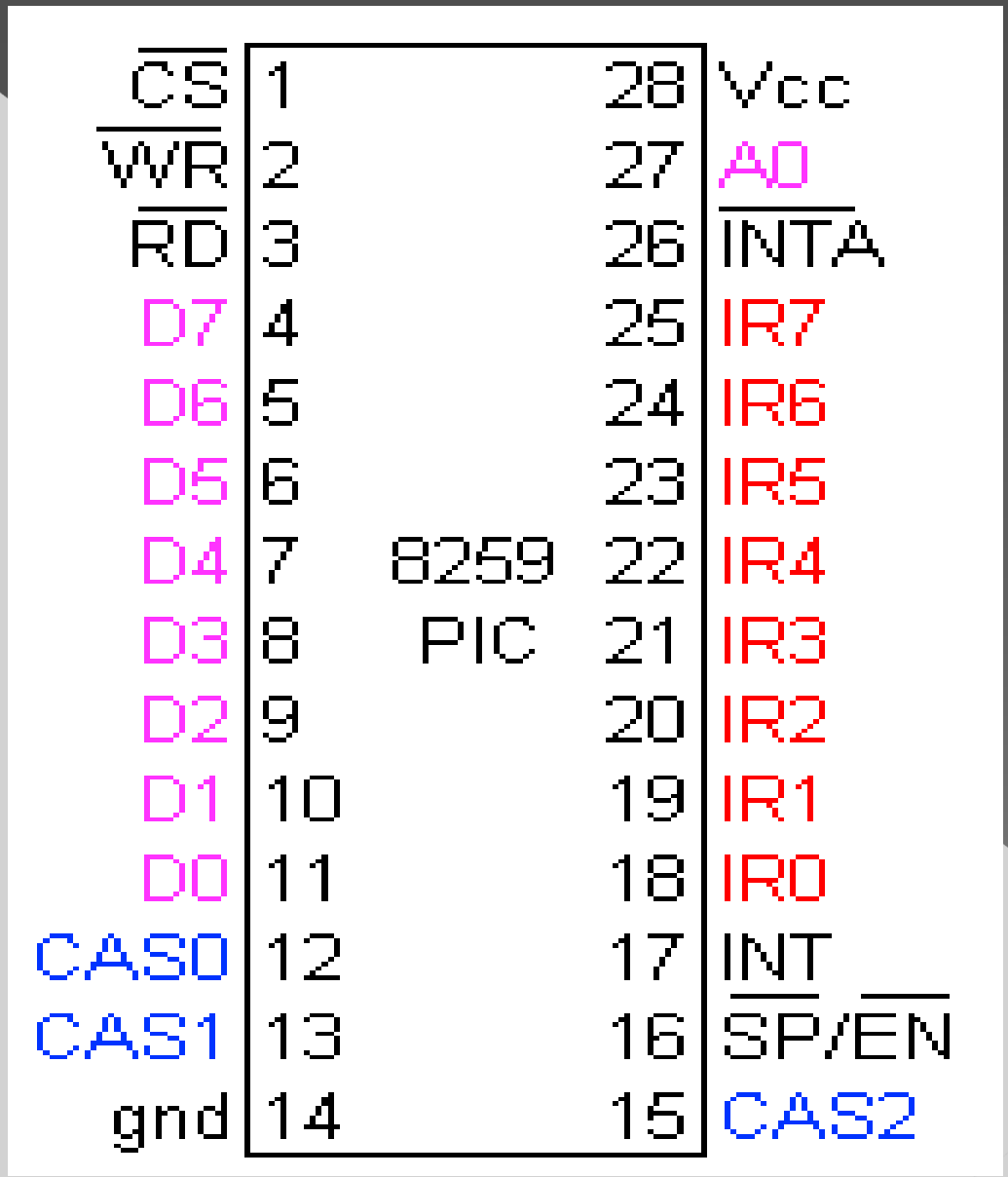
- The 8259A is a programmable interrupt controller designed to work with Intel 8080A,8085A,8086 And 8088 microprocessors.
- It works as an overall manager in an interrupt driven system environment.
- It is used when several I/O devices transfer data using interrupt and they are to be connected to the same interrupt level of the microprocessor.

Features of 8295A Programmable Interrupt Controller

- It can handle 8 external interrupts . This is equivalent to providing eight interrupt pins on the processor in place of one INTR/INT pin.
- The starting address of the interrupts service routine can be vectored to any location in the memory map. This eliminates the major drawback of 8085 interrupt in which all the interrupts are vectored to memory location on page 00h.

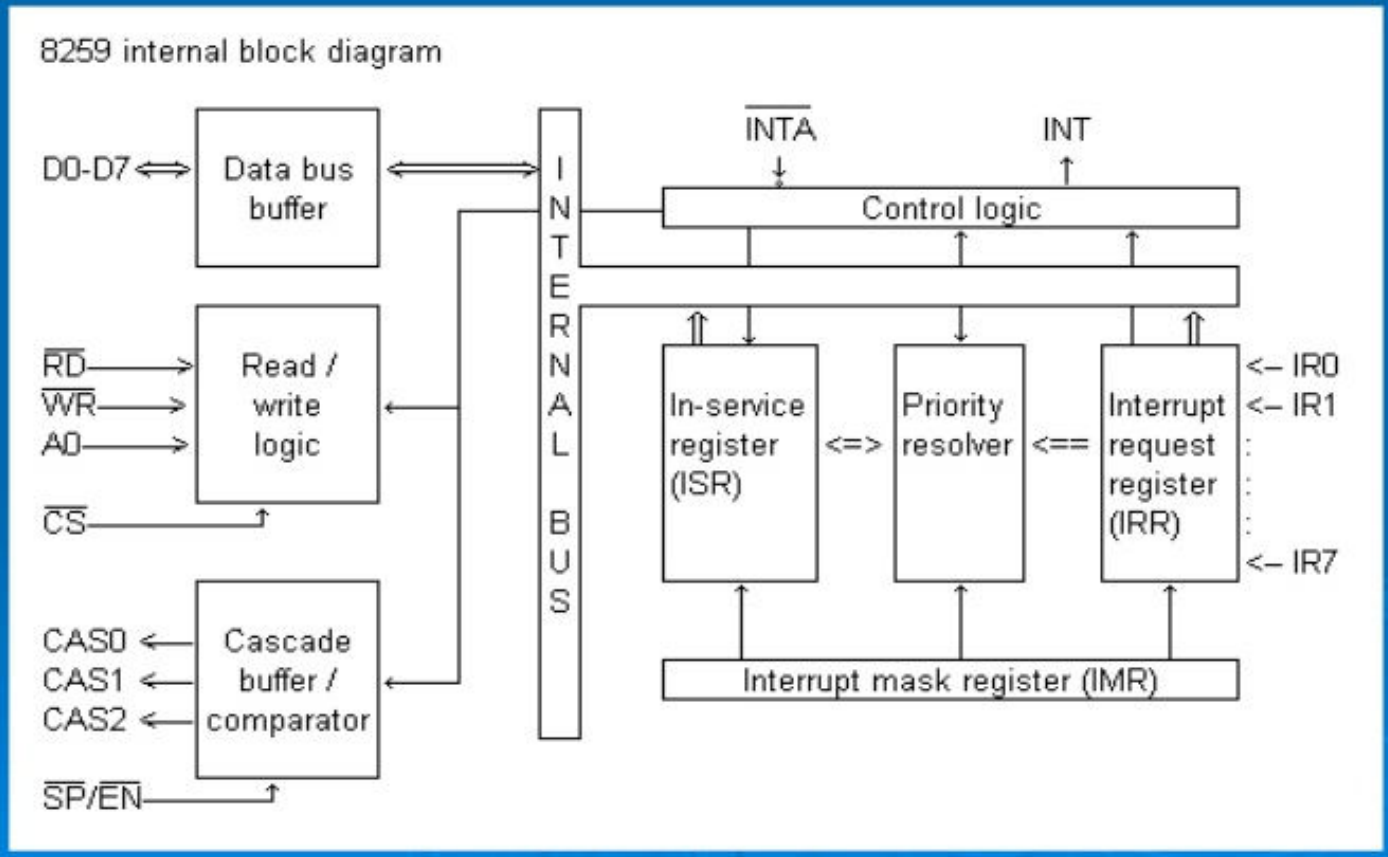
- Resolve eight levels of interrupt priorities in a variety of modes.
- Mask each request individually.
- Read the status of pending interrupts in service interrupts and masked interrupts.
- Be set up to accept either the level triggered or edge triggered interrupt request.
- The 8259 can be cascaded in a master slave configuration to handle 64 interrupt inputs.

PIN DIAGRAM OF 8259A



- The 8259 is a programmable interrupt controller which uses NMOS technology.
- It is available in 28 pin plastic dial in line package (DIP).
- It requires one power supply of 5+ V but does not require any internal or external clock.
- A single PIC can accept interrupt requests from eight I/O devices, resolve priority among them and communicate to the microprocessor.
- Interrupt requests from all the I/O devices can individually be masked and a suitable priority mode can be selected by programming.
- Built in expandability has also been provided to cascade 9 such Programmable Interrupt Controller devices (8259s) to serve up to 64 I/O devices

8259A Block Diagram (Repeat)



- The 8259A contains four sections:
- 1. Data bus buffer.
- 2. Read/write control logic section.
- 3. Cascade buffer/comparator section.
- 4. Interrupt and control logic section.

- 1. Data bus buffer : This is a tri-state bidirectional 8-bit data bus buffer used to interface the 8259A to data bus of 8085. The control words and status information are transferred through this data buffer.
- 2. Read/Write control logic section : The function of this read/write control logic section is to accept the commands from the MPU.
- It contains the initialization command word (ICW) registers and the operation command word (OCW) registers which store the various control formats for device operation.
- This section also accepts Read commands from the MPU to read status words.
- The four pins are connected to a block which are:

- CS (chip select) : This pin is active low chip select terminal. When it goes low the 8259A is selected for interrupts service.
- RD : This is an active low signal and of the interrupt request register (IRR), In service register , the interrupt mark register(IMR) or the interrupt level on the data bus.
- WR : This is an active low signal and it enable the write operation.. A low on this interrupt enables the MPU to write initialization control word (ICW) and operation command word (OCW) to the 8259A
- A0 : This is the input signal used in conjunction with the signals WR and RD to write the commands into the various status registers of the device. This terminal is directly connected to A0 address lines. When the address line A0 is at logic 0. the controller is selected to write a command or read a status.

- 3. Cascade buffer/comparator section : This block is used to expand the number of interrupt levels up to 64 levels by cascading two or more 8295A. In such cases one 8259A acts as the master and the others acts as slaves. The necessary control signals for cascade operations are generated with this block. A high on the slave program pin selects 8259A master and a low to this pin selects 8259A slave. For a master, the pin CAS0-CAS2 are outputs, and for slave CAS0-CAS2 are input pins.

- 4. Interrupt and control logic section
- > Interrupt request register (IRR)
- > In-Service register (ISR)
- > Priority Resolver
- > Interrupt Mask Register (IMR)
- > Control Logic Section

Interrupt Request Register (IRR)

- The IRR is used to store all the interrupt levels which are requesting services. It has 8 interrupt lines IR0 to IR7. when any of these lines become high, the corresponding mask bit is checked and if it is enabled, then the corresponding bit in the interrupt request register is set.

In-Service Register (ISR)

- The ISR is used to store information of all the interrupt levels which are currently being serviced.

Interrupt Mask Register (IMR)

- The IMR stores the bits of the interrupt lines to be masked.
- The IMR operates on the ISR.
- This registered can be programmed by an operation command word (OCW) to store the bit of the interrupt lines to be masked .
- An interrupt which is masked by software will not be recognized and serviced even if it sets the corresponding bits in the IRR

Priority Resolver

- It determines the priorities of the bits set in the IRR.
- The bit corresponding to the highest priority interrupt is set in the ISR during the INTA input is consider for service, but it will reject a lower priority interrupt.
- The priority resolver does the job of judging whether to allow another interrupt to be executed in the middle of executing one interrupt service routine.

Control Logic Section

- After the interrupt request priorities are resolved by the priority resolver , control logic sends an interrupt signal through its INT signal to the MPU.
- This terminal INT is connected to the INTR terminal of the microprocessor.
- The microprocessor responds to this request by sending the interrupt acknowledge signal INTA to the input terminal INTA of the 8259A.

Interrupt Operation

- To implement interrupts, the Interrupt Enable Flip Flop in the Microprocessor is enabled by writing the EI instruction, and the 8259A is initialized by writing control words in the control register. After the 8259A is initialized , the following sequence of event occurs when one or more interrupt request lines go high:

- 1. The IRR stores the request.
- 2. The priority resolver checks the IRR for interrupt requests, the IMR for making bits, and the ISR for interrupt request being served. It resolves the priority and sets the INT high when appropriate.
- 3. The MUP acknowledged the interrupt by sending INTA.
- 4. After the INTA is received , the appropriate priority bit in the ISR is set to indicate which interrupt level is being served and then the opcode for the CALL institution is placed on the data bus.

- 5. When the MPU decodes the CALL instruction ,it places two more INTA signals on the data bus.
- 6. When the 8259A received the second INTA it place the low order byte of the CALL address on the data bus. The address is the vector memory location for the interrupt.
- 7. During the third INTA pulse, the ISR bit is reset automatically .
- 8. The program sequence is transferred to the memory location specified by the CALL indtruction.

Priority Modes

- Many types of priority modes are available under software control in the 8259A and they can be changed dynamically during the program by writing appropriate command words.

1. Fully Nested Mode (FNM)

- The FNM is the general purpose mode in which all interrupt requests are arranged from the highest to lowest priority level.
- This is the default mode setting after initialization.
- The 8259 continues to operate in FNM until the mode is changed by OCWs.

2. Automatic Rotation Mode

- In this mode a device after being serviced receives the lowest priority.

- 3. Specific Rotation Mode

This mode is similar to the automatic rotation mode, except that the user can select any IR for the lowest priority , thus fixing all other priorities.

End Of Interrupt

- After the completion of an interrupt service, the corresponding ISR bit needs to be reset to update the information in the ISR. This is called the End-of-Interrupt (EOI) command.
- 1. Non specific EOI command: When this command is sent to 8259A, it resets the highest priority ISR bit.
- 2. Specific EOI command: This command specifies which ISR bit to reset.
- 3.Automatic EOI: In this mode no command is necessary. The major drawback of this mode is that, the ISR does not have information on which IR is being serviced.